

CLAIMS

- 1 1. A method of relieving charge accumulations from non-volatile
2 memory structures on dies on a wafer, including:
3 applying an electrical erase signal to the non-volatile memory structures on the
4 dies; and
5 baking the wafer under conditions sufficient to diffuse charges resulting from
6 the erase signal.
- 1 2. The method of claim 1, wherein the electrical erase signal produces a
2 negative gate channel erase by Fowler-Norheim tunneling.
- 1 3. The method of claim 1, wherein the electrical erase signal produces a
2 negative gate source side erase by Fowler-Norheim tunneling.
- 1 4. The method of claim 1, wherein the electrical erase signal produces a
2 hot hole erase.
- 1 5. The method of claim 4, wherein the hot hole erase includes biasing
2 either a source or drain of the memory cells.
- 1 6. The method of claim 4, wherein the hot hole erase includes biasing
2 both of a source and drain of the non-volatile memory cells.
- 1 7. The method of claim 1, wherein the non-volatile memory structures
2 include an ONO structure.
- 1 8. The method of claim 7, wherein the electrical erase signal produces a
2 hot hole erase.
- 1 9. The method of claim 8, wherein the hot hole erase includes biasing
2 either a source or a drain of the memory cells.
- 1 10. The method of claim 8, wherein the hot hole erase includes biasing
2 both a source and a drain of the non-volatile memory cells.
- 1 11. The method of claim 1, wherein the baking includes heating the wafer
2 to between 80 and 150 degrees Celsius.
- 1 12. The method of claim 1, wherein the baking includes heating the wafer
2 to between 150 and 250 degrees Celsius.

1 13. The method of claim 1, further including determining an erasure state
2 of the memory cells and repeatedly applying an additional electrical erase signal
3 until a predetermined erasure state is achieved.

1 14. A method of relieving charge accumulations from ONO non-volatile
2 memory structures on dies on a wafer, including applying an electrical erase
3 signal to the ONO non-volatile memory structures on the dies prior to subdividing
4 the wafer into the dies.

1 15. The method of claim 14, further including baking the wafer after
2 applying the electrical erase signal under conditions sufficient to diffuse charges
3 resulting from the electrical erase signal.

1 16. The method of claim 15, wherein the baking includes heating the wafer
2 to between 80 and 150 degrees Celsius.

1 17. The method of claim 15, wherein the baking includes heating the wafer
2 to between 150 and 250 degrees Celsius.

1 18. The method of claim 14, wherein the electrical erase signal produces a
2 negative gate channel erase by Fowler-Norheim tunneling.

1 19. The method of claim 14, wherein the electrical erase signal produces a
2 negative gate source side erase by Fowler-Norheim tunneling.

1 20. The method of claim 14, wherein the electrical erase signal produces a
2 hot hole erase.

1 21. The method of claim 20, wherein the hot hole erase includes biasing
2 either a source or a drain of the memory cells.

1 22. The method of claim 20, wherein the hot hole erase includes biasing
2 both a source and a drain of the non-volatile memory cells.

1 23. The method of claim 22, further including determining an erasure state
2 of the memory cells and repeatedly applying an additional electrical erase signal
3 until a predetermined erasure state is achieved.